Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for manufacturing a device including an n-type device and a p-type device, comprising:
forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device;
adjusting the shallow-trench-isolation oxide corresponding to at least one of the n-type device and the p-type device such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is different from a thickness of the shallow-trench-isolation oxide adjacent to the p-type device; and
forming a strain layer over the semiconductor substrate.

[c2] The method of claim 1, wherein the strain layer comprises an etch stop nitride film.

[c3] The method of claim 1, wherein the strain layer is one of a compressive strain layer or a tensile strain layer.

[c4] The method of claim 1, wherein the step of adjusting comprises forming a pad nitride with a first thickness for the n-type device and forming a pad nitride with a second thickness for the p-type device such that the first thickness is different from the second thickness.

[c5] The method of claim 4, wherein the first thickness is smaller than the second thickness.

[c6] The method of claim 4, wherein the first thickness is greater than the second thickness.

[c7] The method of claim 1, wherein the step of adjusting comprises covering the n-type transistor while exposing the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the n-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the p-type device.

[c8] The method of claim 7, wherein the oxide etching chemical includes HF (hydrofluoric acid).

[c9] The method of claim 1, wherein the step of adjusting comprises covering the p-type transistor while exposing the n-type transistor and the semiconductor substrate to at least one oxide etching chemical, such that a thickness of the shallow-trench-isolation oxide adjacent to the p-type device is greater than the thickness of the shallow-trench-isolation oxide adjacent to the n-type device.

[c10] The method of claim 9, wherein the oxide etching chem-

ical includes HF.

[c11] The method of claim 1, wherein the step of forming a strain layer comprises forming at least one of a SiGe, Si_3N_4, SiO_2 and Sio_xN_y layer on the semiconductor substrate.

[c12] The method of claim 1, wherein the step of forming a shallow-trench-isolation oxide (STI) isolating the n-type device from the p-type device comprises forming the shallow-trench-isolation oxide at a distance of about 1500 Angstromsor less from the adjacent n-type device or p-type device.

[c13] The method of claim 1, wherein the thickness of the shallow-trench-isolation oxide of one of the n-type device or the p-type device is about 300 Angstroms to about 1000 Angstromsless than the shallow-trench-isolation oxide of the other of the n-type device or the p-type device.

[c14] A method for manufacturing a device including an n-type device and a p-type device, comprising:
forming a boundary for the n-type device and the p-type device;
adjusting a height of the boundary such that a boundary adjacent to the n-type device is at a level which is differ-

ent from a level of a height of a boundary adjacent to the p-type device; and

forming a strain layer over the semiconductor substrate.

[c15] The method of claim 14, wherein the strain layer comprises a compressive strain layer or a tensile strain layer.

[c16] The method of claim 15, wherein:

the strain layer is a tensile strain layer, and

the height of the boundary adjacent to the n-type device is lower than the height of the boundary adjacent to the p-type device.

[c17] The method of claim 16, wherein:

the strain layer is a compressive strain layer, and

the height of the boundary adjacent to the p-type device is lower than the height of the boundary adjacent to the n-type device.

[c18] A semiconductor device, comprising:

a strain layer formed over n-type transistors and p-type transistors formed on a silicon substrate; and

a shallow-trench-isolation oxide around each of the n-type transistors and the p-type transistors, wherein an upper surface of the shallow-trench-isolation oxide of the n-type transistors is at a level than a level of an upper surface of the shallow-trench-isolation oxide of the

p-type transistors.

[c19] The device of claim 18, wherein the strain layer comprises a compressive strain layer.

[c20] The device of claim 19, wherein an upper surface of shallow-trench-isolation oxide of the n-type transistor is higher than an upper surface of the silicon substrate.

[c21] The device of claim 20, wherein the upper surface of the shallow-trench-isolation oxide of the n-type transistor is about 300 Angstroms to about 1000 Angstroms higher than an upper surface of the silicon substrate.

[c22] The device of claim 21, wherein an upper surface of the shallow-trench-isolation oxide of the p-type transistor is between being substantially planar to the upper surface of the silicon substrate to about 1000 Angstroms below the upper surface of the silicon substrate.

[c23] The device of claim 18, wherein the strain layer comprises a tensile strain layer.

[c24] The device of claim 23, wherein an upper surface of the shallow-trench-isolation oxide of the p-type transistor is higher than an upper surface of the silicon substrate.

[c25] The device of claim 24, wherein the upper surface of the shallow-trench-isolation oxide of the p-type transistor

is about 300 Angstroms to about 1000 Angstroms higher than an upper surface of the silicon substrate.

[c26] The device of claim 25, wherein an upper surface of the shallow-trench-isolation oxide of the n-type transistor is between being substantially planar to the upper surface of the silicon substrate to about 1000 Angstroms below the upper surface of the silicon substrate.

[c27] The device of claim 18, wherein the strain layer has a thickness of about 250 Angstroms to about 1500 Angstroms.

[c28] The device of claim 18, wherein compressive stresses of about 100 MPa to about 3 GPa exist within the channel of the p-type device.

[c29] The device of claim 18, wherein tensile stresses of about 100 MPa to about 3 GPa exist within the channel of the n-type device.

[c30] The device of claim 18, wherein the shallow-trench-isolation oxide of each of the n-type transistor and the p-type transistor is about 200 Angstroms to about 1500 Angstroms from a corresponding gate of the n-type transistor or a corresponding gate of the p-type transistor, respectively.